CLAIMS

1. A method for testing a unit comprising:

receiving at least one compressed test vector by the unit;

decompressing at least one compressed test vector; and

generating at least one output from the unit based at least in part on the testing of the unit with the decompressed test vector.

2. The method of claim 1 further comprising:

compressing at least one output by the unit; and

forwarding the compressed output to a test platform.

3. The method of claim 1 wherein decompressing at least one compressed test vector comprises bypassing the decompression if the test vector does not efficiently compress.

4. The method of claim 2 wherein compressing at least one output comprises bypassing the compression if the output does not efficiently compress.

5. The method of claim 1 wherein the test vector is either one of a functional vectors, parametric vectors, automatic pattern generation (ATPG) vectors, initialization vectors, and reset vectors.

6. The method of claim 1 wherein receiving at least one compressed test vector comprises loading the compressed test vector with either a single pin of the unit in a serial manner or a plurality of pins in a parallel manner.

7. The method of claim 1 wherein the unit is either one of a system on a chip (SoC), an integrated device, or a chipset.

8. The method of claim 1 wherein the test platform is either one of a workstation, automatic test equipment, network analyzer, and a logic analyzer.

9. A system comprising:

a vector generation logic to generate a plurality of test vectors; and

a device under test, coupled to the vector generation logic, the system to compress at least one of the plurality of test vectors and to decompress the compressed test vectors when applied to the device under test, and to compress at least one of the plurality of outputs generated by the device under test in response to the decompressed test vector or vectors.

10. The system of claim 9 further comprising an analysis logic to receive the decompressed plurality of output or outputs.

11. The system of claim 9 wherein the plurality of test vectors is either one of a functional vectors, parametric vectors, automatic pattern generation (ATPG) vectors, initialization vectors, and reset vectors

12. The system of claim 9 wherein the device under test is either one of a system on a chip (SoC), an integrated device, or a chipset.

13. The system of claim 9 wherein the vector generation logic is either one of a workstation, automatic test equipment, network analyzer, and a logic analyzer.

14. The system of claim 10 wherein the analysis logic is either one of a workstation, automatic test equipment, network analyzer, oscilloscope, and a logic analyzer.

15. An apparatus comprising:

an input port to receive at least one compressed test vector;

a decompression logic to decompress the compressed test vector; and

the apparatus to generate at least one output based at least in part on the decompressed test vector

16. The apparatus of claim 15 wherein the input port is a single pin or a plurality of pins that receive the test vector(s).

17. The apparatus of claim 15 wherein the decompression logic supports a delta method decompression protocol.

18. The apparatus of claim 15 wherein the apparatus is either one of a system on a chip (SoC), an integrated device, or a chipset.

19. The apparatus of claim 15 wherein test vector(s) is either one of a functional vectors, parametric vectors, automatic pattern generation (ATPG) vectors, initialization vectors, and reset vectors.

20. The apparatus of claim 15 wherein the apparatus comprises a compression logic to compress the output(s).